ABSTRACT

Provided is a data input unit of a synchronous semiconductor memory device comprising: means for generating a rising edge signal and a falling edge signal at a rising edge and a falling edge of a data strobe signal DQS to be input; means for generating a second falling edge signal whenever two falling edge signals are generated in response to the data strobe signal; a data transforming means for dividing input data into four and latching the four divided data in response to the rising edge signal and falling edge signal, and then latching again the four divided data in response to the second falling edge signal; and a global input/output signal generator for transmitting the data from the data transforming means to a global input/output line in response to a strobe clock.